AMENDMENT OF THE CLAIMS

1. (Currently Amended) An apparatus for reducing power consumption by a clock and data recovery loop circuit, comprising:

a flywheel to monitor adjustments made in a phase of a sampling clock by a phase controller, the sampling clock being generated to sample bit values from a data signal, and to modify the adjustments in the phase of the sampling clock to track a phase of the data signal; and

a loop latency controller to monitor the modifications of the adjustments to the phase of the sampling clock, to determine the existence of spread spectrum clocking based upon a pattern of the modifications, and, in response, to adapt a stage of the clock and data recovery loop circuit to operate with less power consumption.

2. (Original) The apparatus of claim 1, wherein the loop latency controller determines a frequency select signal to modify an operating frequency for the stage.

3. (Original) The apparatus of claim 1, wherein the loop latency controller couples with a multiplexer to select a clock frequency for the stage.

4. (Original) The apparatus of claim 1, wherein the loop latency controller couples with a voltage controller to reduce an operating voltage for the stage.

5. (Currently Amended) The apparatus of claim 1, wherein the loop latency controller outputs a control signal to merge the stage with a second stage of the clock and data recovery loop circuit.

6. (Original) The apparatus of claim 5, wherein the control signal comprises a latch control signal to bypass a latch coupled between an output of the stage and an input of the second stage.

7. (Original) The apparatus of claim 5, wherein the control signal comprises a logic control signal to coordinate a mergence of the stage with the second stage.

8. (Original) The apparatus of claim 1, wherein the loop latency controller outputs a control signal to deactivate the stage and activate a second simpler stage to perform a substantially similar function as the stage.

9. (Original) The apparatus of claim 1, wherein the stage comprises a multiple-state, rotator state machine and the second stage comprises a second rotator state machine, wherein the multiple-state, rotator state machine has more states than the second rotator state machine.

10. (Currently Amended) A method for reducing power consumption by a clock and data recovery loop circuit, the method comprising:

monitoring adjustments made in a phase of a sampling clock by a phase controller, the sampling clock being generated to sample bit values from a data signal;

modifying the adjustments in the phase of the sampling clock to track a phase of the data signal;

monitoring the modifications of the adjustments in the phase of the sampling clock;

determining the existence of spread spectrum clocking based upon a pattern of the modifications; and

adapting a stage of the clock and data recovery loop circuit in response to determining the existence of spread spectrum clocking to operate with less power consumption.

11. (Original) The method of claim 10, wherein adapting the stage comprises selecting a clock signal to modify an operating frequency for the stage.

12. (Original) The method of claim 10, wherein adapting the stage comprises determining a voltage select signal to reduce an operating voltage for the stage.

13. (Currently Amended) The method of claim 10, wherein adapting the stage comprises merging the stage with a second stage of the clock and data recovery loop circuit.

14. (Original) The method of claim 13, wherein merging the stage comprises bypassing a latch coupled between an output of the stage and an input of the second stage.

15. (Currently Amended) The method of claim 10, wherein adapting the stage comprises deactivating the stage and activating a second simpler stage, wherein the second simpler stage performs a substantially similar function as the stage.

16. (Currently Amended) A clock and data recovery loop circuit, comprising:

a clock generator to generate a sampling clock;

sampling circuitry to sample values for a bit from a data signal based upon the sampling clock;

comparison circuitry to compare the values for the bit to generate a comparison signal indicative of a difference between the phase of the sampling clock and the phase of the data signal;

a phase controller to adjust the phase of sampling clock in response to the comparison signal;

a flywheel to monitor adjustments in the phase of the sampling clock by the phase controller and to modify the adjustments in the phase of the sampling clock to track the phase of the data signal; and

a loop latency controller to monitor the modifications of the adjustments in the phase of the sampling clock, to determine the existence of spread spectrum clocking based upon a pattern of the modifications, and, in response, to adapt a stage of the clock and data recovery loop circuit to operate with less power consumption.

17. (Currently Amended) The clock and data recovery loop circuit of claim 16, wherein the loop latency controller generates a frequency select signal to modify an operating frequency for the stage.

18. (Currently Amended) The clock and data recovery loop circuit of claim 16, wherein the loop latency controller couples with a voltage controller to modify an operating voltage for the stage.

19. (Currently Amended) The clock and data recovery loop circuit of claim 16, wherein the loop latency controller outputs a control signal to merge the stage with a second stage of the clock and data recovery loop circuit.

20. (Currently Amended) The clock and data recovery loop circuit of claim 16, wherein the loop latency controller outputs a control signal to deactivate the stage and activate a second simpler stage to perform a substantially similar function as the stage.